Donald Gerard Polak

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Summary

Electronics engineer with a substantial record of achievements in several different areas of server and telecommunications, design, test, and software disciplines. Well known for being a team player, with a history of innovation while adhering to standards and industry best practices. Possess a proven ability to learn hardware and software systems, languages, and techniques for advanced technologies using self-paced research and study. Customer oriented individual who has frequently been rewarded for cost effective, defect free, on-time solutions that exceed objectives.

Patents and Publications

- Patent US-20150074312 A1 September 9, 2013. “Multi-Channel Universal Serial Bus (USB) to Subrate Channel Systems and Methods”.
- Patent US-20150120982 October 24, 2013. “Multi-Channel Universal Serial Bus (USB) to Subrate Channel Systems and Methods” (additional disclosures).
- "Fastlane: An Inexpensive Local Network for ATE Data Collection", Electronics Test, October 1983.
- "Memory pointers cut access time for relational database", Electronics Design, March 31, 1983
- “Solving 74LS163 In-Circuit Testability Problems, Electronics Test, February 1982

Skills

- Digital, analog, and mixed signal electronic hardware design and documentation preparation including design specifications, RFQs, schematic capture, printed circuit board (PCB) layout, and mechanical and assembly drawings; conforming to DFx disciplines and best practices.
- FPGA and CPLD design in Verilog, VHDL, and other HDL languages, using devices from Altera, Xilinx, Lattice Semiconductors, Cypress, and Micro-Semi; that adhere to design for reuse standards. Extensive simulation experience using a variety of simulator software.
- Embedded system architectural, hardware and layout design including SERDES, 1 and 10 gigabit Ethernet (GbE), RGMII, SGMII, SPI, eSPI, I^2C, USB, SATA, DDR, and eMMC.
- Test development including hardware, software, ATE program, fixture, and mechanical design for high-volume production test solutions including JTAG, HALT, and FIT testing.
- Root causal analysis, and defect prevention process training and experience.
- Software, operating system, and embedded system code development using C, Javascript, PERL, PASCAL, and assembler. LINUX scripting experience using C-shell and BASH.
- Digital and automatic central office design, test, installation and maintenance.

Experience

LENOVO USA INCORPORATED, Morrisville, NC 27560 2014 – 2015
Staff Engineer

Design and verify products for use in high end servers.

- Designed an embedded microsystem for chassis management, two 10 GbE KR to copper interfaces, a PCIE expansion module, a SAS/SATA interposer, and three test cards for next generation servers. This activity provided guide designs to other engineers that allowed Lenovo to move ahead of its competitors in projected release dates for INTEL “Purley” and “Skylake” based servers.

- Performed building block functional verification (BBFV) of third generation baseboard management controller (BMC), DDR4, I^2C, and serial interfaces; including WINAPI development of test utilities using GCC and MINGW. These test utilities were designed to support future testing and debug of the product, avoiding future development costs.

IBM CORPORATION, Research Triangle Park, NC 27709 2011 – 2014
Hardware Design Engineer

Design modules for management of servers and develop proof of concept (POC) prototypes for new products. Provide customer defect and component obsolescence solutions for chassis management products.

- Conceived, composed, and simulated FPGA code for a patented Universal Serial Bus (USB), version 2.0, channel bank for multiple, feature rich, I^2C master/slave interfaces; which includes a ULPI interface and a USB 2.0 compliant serial interface engine (SIE). This project allows IBM to avoid future development costs and creates opportunities to consider cheaper alternatives to application specific BMCs.
- Developed architectural proposals and supplied vendor specifications for next generation, server management hardware, enabling a joint venture between IBM and another technology company.
- Designed, debugged, and provided user support for chassis management hardware including EMMC, USB, RGMII, SGMII, SERDES, GbE, I^2C, DDR2, and DDR3 interfaces; and switch mode power converters., enabling IBM to increase customer satisfaction.
- Provided software utility development for internal and vendor support of PureSystem™ hardware in C language and BASH scripting, speeding the release of the product.
- Engaged in mentoring for other, less experienced engineers.

COMPUTER TASK GROUP, Morrisville, NC 27560 2010 – 2011
Contract Hardware Designer (Assigned to IBM)

Support introduction of the PureSystem™ product line. Provide customer defect and component obsolescence solutions for the BladeCenter™ product line.

- Assisted in design, bring up, test, debug, and user support of chassis management hardware. Designed DDR3 and RGMII terminations, VREF/VTT supplies, EMMC, TPM, and cold restart circuits for the chassis management module (CMM).
- Developed software algorithm and C program code used by IBM and all IBM vendors for generation of the CRC-32 check in vital product data using Galois fields.
- Composed new CPLD code for the Advanced Managed Module (AMM) used in the BladeCenter™ product line to resolve long standing defects.

NORTEL NETWORKS, Research Triangle Park, NC 27709 1978 – 2009
Senior Design Engineer, 2003 – 2009

Perform electronic and mechanical design of circuit boards and subassemblies for new products, and cost reduction, manufacturing support, component obsolescence resolution and defect solutions for existing products.

- Performed reverse engineering and developed alternatives for part consolidation or replacement. Created HDL code for 8085A microprocessor, 8251 USART, 8254A timer, framers, de-framers, 1.3 gigabit per second switching fabric, embedded systems interface electronics, DSP-based alarm systems, and other applications, in many case achieving over 50% cost reduction.

- Wrote software, including assemblers and real-time operating systems, for embedded systems and systems support in C and assembly languages, avoiding additional software development expenses.
- Designed PCB layouts to speed product releases.
- Developed and executed design verification and manufacturing test plans.
- Mentored other design engineers.

Design Engineer, 1999 – 2003

Perform defect resolution, manufacturing sustainment, and cost reduction design of digital telephone switching equipment circuit packs.

- Re-designed or modified over 20 circuit packs, including PCB layouts, to resolve defects and component obsolescence issues.
- Served as component obsolescence prime for the entire product line.
- Devised and executed design verification test cases.

Additional Experience

Product Engineer, Test Engineer, Software engineer, Staff sergeant USMC

- Managed defect prevention projects and teams.
- Created software using PERL, HTML, JAVASCRIPT, C, and assembler for a web-based client/server system for fault reporting, project management of the fault resolution; root cause analysis of the fault, and the defect prevention process. Composed an instrument-based, object-oriented, test language interpreter, DSP based measurement analysis software, a viewer/translator for HPGL files, interfaces to integrate programmable logic controllers into data collection and analysis systems, and custom design tools. Designed a software system (FASTLANE), which was widely used as a basis for modern quality test data collection, control, and analysis systems), to implement factory-wide, data collection and analysis and provide local area networking.
- Designed automatic test equipment (ATE) hardware, including complete test systems using both VXI and GPIB based equipment.
- Designed electrical and mechanical assemblies that provided a two hundred percent increase in production test throughput.
- Designed hardware interfaces to incorporate automatic central office equipment into a tactical environment

Education

- Advanced DSP with a Few Tears, and DSP Without Tears, Right Brain Technologies
- Error Correcting Codes and Reed Solomon Codes, UCCE
- Root Cause Analysis, Department of Technical Training, Northern Telecom
- Digital telephony engineering courses, Department of Technical Training, Northern Telecom
- DMS-1 Systems Course, Department of Technical Training, Northern Telecom
- Basic Telephony, Department of Technical Training, Northern Telecom
- Automatic Central Office Repair Course, US Army Signal School
- Staff Non-Commissioned Officers Academy, Camp Lejeune, NC
- KW26C Cryptographic Repair Course, United States Naval Schools Command
- Digital Logic Fundamentals Course, Communications-Electronics School, Marine Corps
- Telephone/Teletype Repair Course, Communications-Electronics School, Marine Corps
- Basic Electronics Course, Communications-Electronics School, Marine Corp